High Resolution Phase Frequency Detectors

BACKGROUND OF THE INVENTION

This appln is a 371 of PCT/CA01/00723 05/24/01 and claims benefit of provisional appln 60/206,579 05/24/00.

1. Field of the invention

This invention is directed to providing high resolution low cost digital phase detectors which can be used in digital phase locked loops (DPLLs) and shall also make possible other replacements of analog circuits by their digital implementations.
The high resolution phase detectors (HRPD) can be used for a wide range of data rates, and for wireless, optical , or wireline transmission and communication systems.

2. Background art

Most of currently used digital phase detectors have resolution limited by a clock cycle time.
While some most advanced digital phase detectors allow higher resolutions which are comparable with propagation delays of clock propagating gates, they have other limitations such as: complex algorithms which are conditioned by propagation delays of detector timing circuits, and dependency of their phase resolution on technological process and power supply variations.

There is a need for digital phase detectors which have simpler algorithms and greater independence versus the propagation delays of the detector timing circuits and the clock propagating gates.

SUMMARY OF THE INVENTION

1. Purpose of the invention

It is an object of present invention to provide digital high resolution phase detectors which are simple and reliable and can be used in variety of communication systems.

2. General description of the invention

Variety of the high resolution phase detectors are described in this document using the same terms which are explained below.
First signal clock f_H is a higher frequency signal which is used to measure time periods corresponding to single or multiple cycles of a lower frequency signal which is called second signal frame fr_L.